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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/791,341	03/01/2004	Cheng-Yen Huang	250606-1060	2419

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EXAMINER	
WENDLER, ERIC J	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/791,341	HUANG, CHENG-YEN	
	Examiner	Art Unit	
	Eric Wendler	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/1/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Search History*.

DETAILED ACTION

Claim Objections

1. **Claim 10** is objected to because of the following informalities: "active" should be changed to --activate--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1-2, and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by the US Patent to Toda (5,010,518).**

4. **Regarding claim 1,** Toda teaches, in Fig. 1D, a memory unit comprising first and second access transistors **DS1 and DS2** coupled to a bit line pair **BL1 and $BL1_{complement}$, or BL2 and $BL2_{complement}$,** wherein the first access transistor comprises a first terminal coupled to one bit line pair, and the second access transistor comprises a first terminal coupled to the other; a latch node coupled between second terminals of the first access transistor and the second access transistor to latch data; and a selection unit **120** having two input terminals coupled to a word line and a flush line, and an output terminal coupled to gates of the first access transistor and the second assess transistor, wherein predetermined information is written to the latch node from the bit line pair

according to activations of the word line or the flush line (see Column 18, lines 32-38).

5. **Regarding claim 2,** Toda teaches, in Fig. 1D, that the selection unit **120** is an OR gate with two terminals coupled to the word line and the flush line (the output line from flush generator **122**) respectively and an output terminal coupled to the gates of the first access transistor and the second access transistor (see Column 18, lines 32-38).

6. **Regarding claim 4,** Toda teaches that the flush line is activated during a flush operation, the first access transistor and the second access transistor are turned on, such that the predetermined information is written into the latch from the bit line pair (see Column 17, lines 57-61, and Column 18, lines 32-38).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

RK 10/12/07

9. **Claims 3, and 5-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over the US Patent to Toda in view of the AAPA (applicant admitted prior art).**

10. **Regarding claims 3 and 9,** Toda teaches all the claimed elements as discussed above but fails to teach that the latch node comprises a first inverter and a second inverter, the first inverter comprises an input terminal coupled to the second terminal of the second access transistor and an output terminal coupled to the second terminal of the first access transistor, and the second inverter comprises an input terminal coupled to the output terminal of the first inverter and an output coupled to the input terminal of the first inverter. The AAPA teaches, in Fig. 2A of the present application, all these elements. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the latch taught in the AAPA in the memory system of Toda because the AAPA refers to the latch as part of a conventional memory unit, and thus may also be used in any memory unit.

11. **Regarding claims 5-8,** Toda teaches all the claimed elements as discussed above, but fails to teach that the memory units are used in a memory module comprised of a plurality of such memory units. The AAPA teaches, on page 2, lines 14-15 of the present application, that a tag memory is comprised of a plurality of SRAM memory units. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the memory units of Toda in a plurality in order to form a memory module or array, as many conventional memories, such as SRAM's, consist of a plurality of memory cells in order to be able to store larger amounts of data.

12. **Regarding claims 11-13,** they encompass the same scope of invention as that of claims 1-10 except they draft the invention in method format instead of

apparatus format. Toda fails to teach a fabricating procedure for a cache memory comprised of his memory units, but teaches the structure of the memory unit. The AAPA teaches, as mentioned in the "Description of the Related Art" section of this application, conventional structures and uses of cache and tag memory. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the memory units of Toda in the cache and tag memory of the AAPA, because the AAPA discloses that the tag memory is comprised of SRAM cells. As mentioned above, the memory units of Toda may obviously be used in the form of a conventional memory, or SRAM. The aspects of the invention contained in claims 11-13 are therefore rejected in method format for the same reasons claims 1-10 were rejected in apparatus format, as set forth in the above paragraphs of the office action.

13. **Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over the US Patent to Toda in view of the AAPA, and further in view of the US Patent to Loo et al (5,845,325).**

14. **Regarding claim 10,** Toda and the AAPA teach all the claimed elements as discussed above but fail to teach a memory unit further comprising a D-type flip-flop (DFF) receiving a synchronizing a flush signal; and a driving buffer coupled to the DFF to activate the flush line according to the flush signal from the DFF. Loo teaches, in Figure 11, a D-type flip-flip receiving and synchronizing a flush signal from the flush address register 52, and a driving buffer 55 coupled to the DFF to activate the flush controls according to the flush signal from the DFF. It would have been obvious to one of ordinary skill in the art at the time the

invention was made to use the DFF and driving buffer of Loo in the memory element of Toda in order to control the flush signal and activate the flush line of the invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Wendler whose telephone number is (571) 272-5063. The examiner can normally be reached on Monday - Friday 8AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

10.7.05

RICHARD ELMS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

EJW
10/6/05